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14EVE12

First Semester M.Tech. Degree Examination, Dec.2015/Jan.2016
Digital VLSI Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. Derive the expression for threshold voltage V_T interms of body effect and surface potential. **(10 Marks)**

b. Calculate the threshold voltage, V_{TO} at V_{SB} = 0 V, for a polysilicon gate n-channel MOS transistor, with the following parameters: Substrate doping density, $N_A = 10^{16}\,cm^{-3}$, Polysilicon gate density (doping), $N_D = 2\times10^{20}\,cm^{-3}$, gate oxide thickness t_{OX} = 400 Å, oxide interface fixed charge density, $N_{OX} = 4\times10^{10}\,cm^{-2}$ and assume $\phi_{F(gate)} = 0.55\,V$, ϵ_{si}, the silicon permittivity as $11.7\times8.85\times10^{-14}$ F/cm and ϵ_{OX}, Permittivity of gate oxide in $3.97\times8.85\times10^{-14}$ F/cm. **(06 Marks)**

c. Why we need scaling and what are its effects in long channel and short channel? **(04 Marks)**

2 a. Derive expression for V_{OH}, V_{OL}, V_{IL} and V_{IH} interms of threshold voltage, for n-type depletion mode load inverter. **(10 Marks)**

b. Calculate the critical voltages V_{OL}, V_{OH}, V_{IL} and V_{IH} and find the noise margins of the depletion load inverter circuit with the following parameters: V_{DD} = 5 V, $V_{TO(driver)} = 1.0\,V$, $V_{TO(load)} = -3.0\ V$, $\left(\frac{\omega}{L}\right)_{(driver)} = 2$, $\left(\frac{\omega}{L}\right)_{(load)} = \frac{1}{3}$, $K_{n(driver)} = K_{n(load)} = 25\ \frac{\mu A}{V^2}$, $\gamma = (0.4)\,V^{\frac{1}{2}}$, $\phi_F = -0.3V$. Assume suitably for iterations values. **(08 Marks)**

c. Differentiate enhancement mode and depletion mode inverters. **(02 Marks)**

3 a. Obtain expression for τ_{PHL} and τ_{PLH} for CMOS inverter interms of V_T and V_{DD} and capacitance. **(10 Marks)**

b. With suitable circuit explain, how to estimate interconnect Parasitics. **(05 Marks)**

c. Show that switching power dissipation of CMOS inverter is given by $P_{avg} = C_{load} V_{dd^2} .f$, where f is the switching frequency. **(05 Marks)**

4 a. Explain briefly with suitable circuit pass transistor in dynamic logic design. **(05 Marks)**

b. Explain how to overcome threshold voltage drop in integrated circuits using voltage bootstrapping technique. **(10 Marks)**

c. Briefly explain cascaded domino CMOS logic circuit for high performance dynamic logic circuit. **(05 Marks)**

5 a. Explain memory structure of SRAM with read and write circuitry with the help of read and write timing diagrams. **(10 Marks)**

b. Explain briefly Flash-memory using NOR-cell configuration. **(06 Marks)**

c. Differentiate DRAM and SRAM. **(04 Marks)**

6 a. What is leakage power dissipation? On what parameters does it depend? **(04 Marks)**

b. Explain briefly adiabatic logic circuit with AND / NAND logic gates. **(10 Marks)**

c. Explain the concept of switching activity with suitable state transition diagram. **(06 Marks)**

7 a. Differentiate BJT, CMOS and BiCMOS. **(06 Marks)**

b. Explain the static behavior of BiCMOS inverter. **(10 Marks)**

c. Realise basic NAND gate with V_A and V_B as inputs by using BiCMOS. **(04 Marks)**

8 Write a short notes on the following:

a. ESD-Protection in I/O circuits.

b. Switching delay in BiCMOS logic circuits.

c. Parametric yield estimation in design for manufacturability.

d. Worst case analysis in manufacturing process. **(20 Marks)**

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